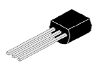
Continental Device India Pvt. Limited
An IATF 16949, ISO9001 and ISO 14001/ISO 45001 Certified Company

SENSITIVE GATE SILICON CONTROLLED RECTIFIER

Passivated, Sensitive Gate Thyristor in TO-92 Package

BT169D
BT169G



TO-92

TO-92
Plastic Package
RoHS compliant

GENERAL DESCRIPTION:

BT169D/G Series SCRs provide high dV/dt Rate with Strong Resistance to Electromagnetic Interface.

FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APLLICATION:

Recommended for use on Residual Current Circuit Breaker, Hair Straightener, Igniter etc.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	BT169D	BT169G	UNIT
Peak Repetitive Off State Voltages	V_{DRM}		400	600	V
	V_{RRM}		400	600	V
Average On-State Current	$I_{T(AV)}$	Half Sine Wave; $T_{lead} \leq 83°C$; See Fig 1.	0.5		A
RMS On-State Current	$I_{T(RMS)}$	All Conduction Angles; See Fig 4 & 5	0.8		A
Non Repetitive Peak On-State Current	I_{TSM}	Half Sine Wave; T_j = 25°C prior to surge;See Fig 2 and 3.			
		t=10ms	8		A
Circuit Fusing Consideration	I^2t	t=10ms	0.32		A^2s
Repetitive rate of Rise of On-State current after Triggering	dI_T/dt	I_{TM}= 2A; I_G = 10mA; dI_G/dt= 100mA/µs	50		A/µs
Peak Gate Current	I_{GM}	t_p=20µs,T_j=110°C	0.2		A
Peak Gate Power	P_{GM}	t_p=20µs,T_j=110°C	0.5		W
Average Gate Power	$P_{G\ (AV)}$	Over any 20ms period	0.1		W
Operating Junction Temperature	T_j		-40 to +110		°C
Storage Temperature Range	T_{stg}		-40 to +150		°C
Thermal resistance from Junction to Case	$R_{th\ (j-c)}$	75			°C/W

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ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX.	
STATIC CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current	I_{DRM}, I_{RRM}	V_D=V_{DRM}, V_R= $V_{RRM,}$ T_j = 25°C	--	--	5	µA
		V_D=V_{DRM}, V_R= $V_{RRM,}$ T_j = 110°C	--	--	100	
Gate Trigger Current	I_{GT}	V_D=12V; R_L=33Ω	--	40	200	µA
Non-triggering gate voltage	V_{GD}	V_D= V_{DRM} , T_J=110ºC	0.2	--	--	V
Latching Current	I_L	V_D=12V; I_{GT}=0.5mA; R_{GK}=1kΩ	--	2	6	mA
Holding Current	I_H	V_D=12V; I_{GT}=0.5mA; R_{GK}=1kΩ	--	2	5	mA
On State Voltage	V_{TM}	I_T=1.1A,tp=380µs,T_j=25°C	--	--	1.5	V
Gate Trigger Voltage	V_{GT}	V_D=12V; R_L=33Ω	--	0.6	0.8	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off- State Voltage	dV_D /dt	V_{DM}=67% $V_{DRM\ (MAX)}$, T_j=110ºC; R_{GK}=1KΩ	200	--	--	V/ms
Gate-controlled turn-on time	t_{gt}	I_{TM}=2A,V_D=V_{DRM}(max); I_G= 10 mA, d_{IG}/d_t = 0.1 A/µs	--	2	--	µS
Commutated turn-off time	t_q	V_{DM}=67% V_{DRM} (MAX), Tj=125ºC; R_{GK}=1KΩ, I_{TM}= 1.6 A; V_R=35V, d_{IT}/dt)M=30A/µs; dV_D/dt = 2 V/µs	--	100	--	µS

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Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

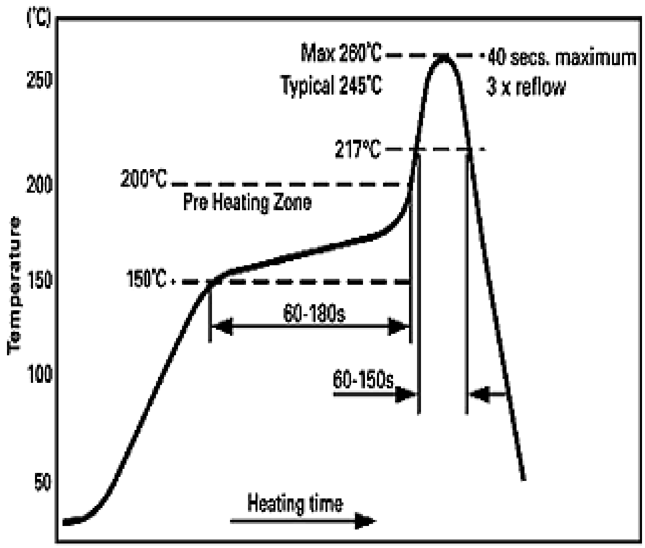
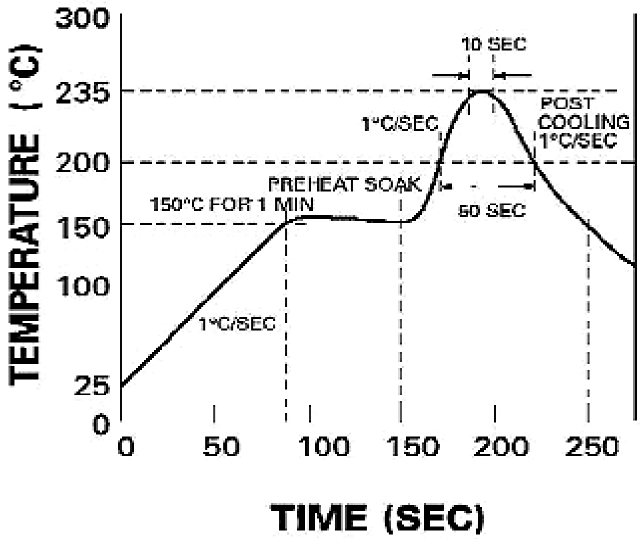


Figure 2



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	150-170°C 60-180 seconds	150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	200°C 30-50 seconds	217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

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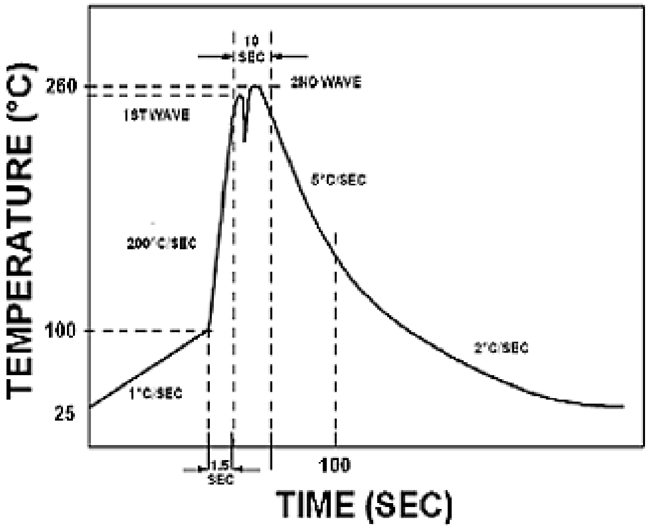
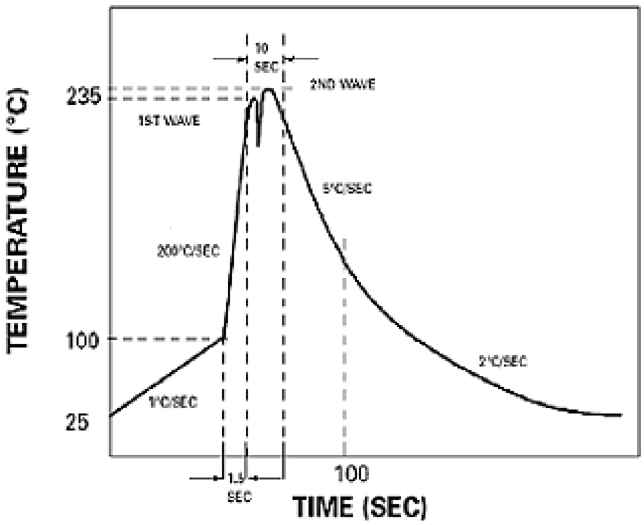
Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

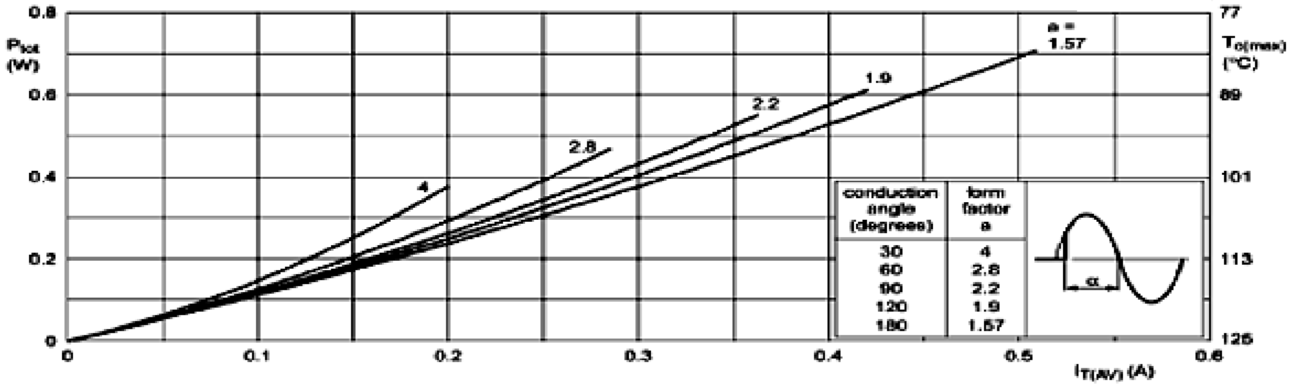


Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

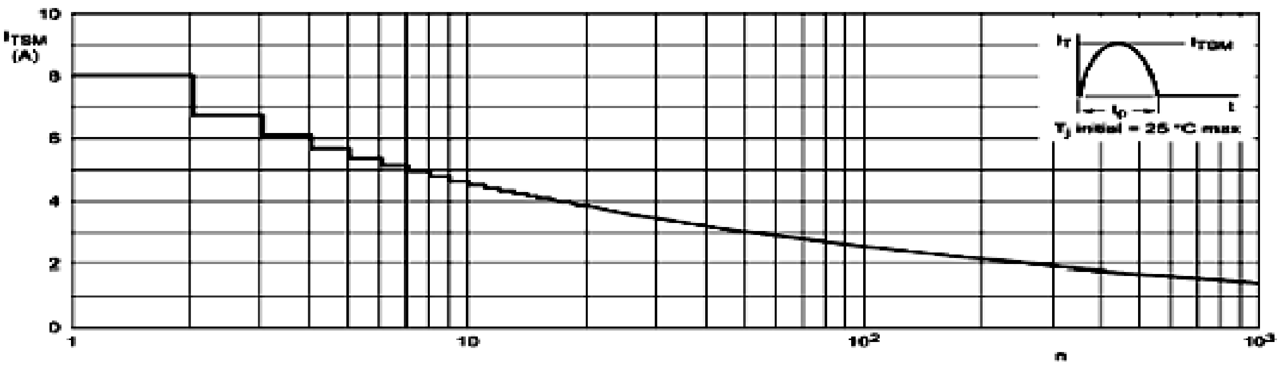
TYPICAL CHARACTERISTICS CURVES

Fig 1: Total Power Dissipation as a function of average on-state current; maximum value



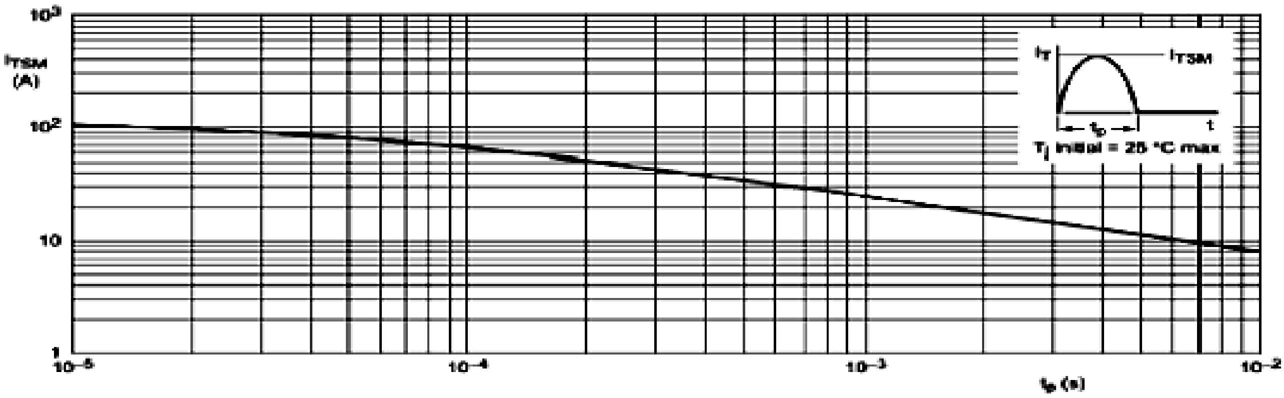
a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

Fig 2: Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum value



f = 50 Hz.

Fig 3: Non-repetitive peak on-state current as a function of pulse width for sinusoidal current; maximum value



$t_p \leq 10$ ms.

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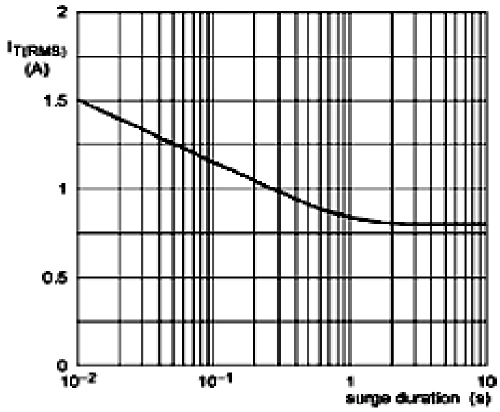
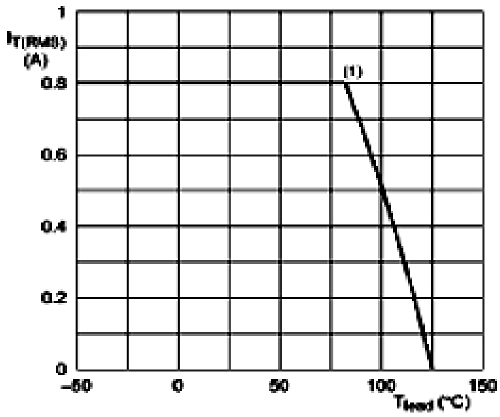
TYPICAL CHARACTERISTICS CURVES

Fig 4: RMS on-state current as a function of surge duration for sinusoidal current



f = 50 Hz; $T_{lead} \leq 83$ °C.

Fig 5: RMS on-state current as a function of lead temperature: maximum values



(1) T_{lead} = 83 °C.

Fig 6: Transient thermal impedance as a function of pulse width

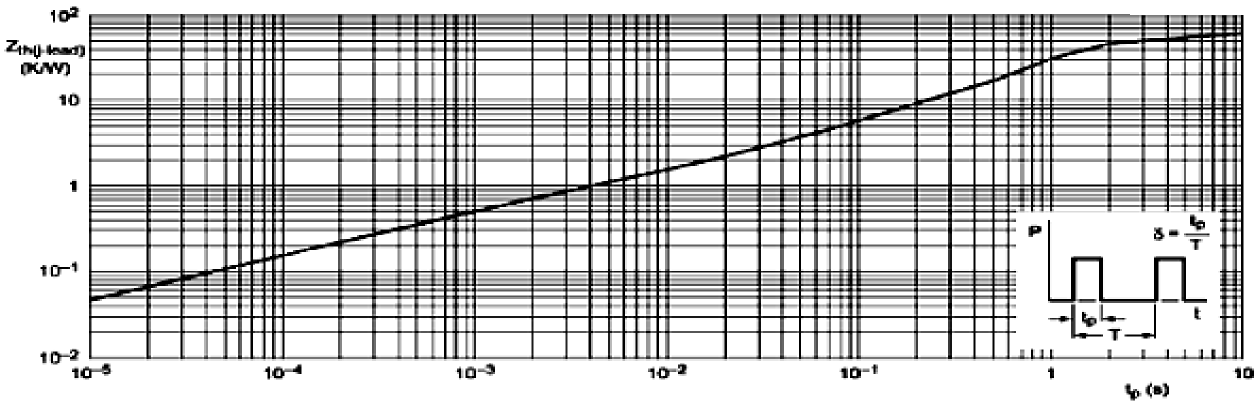


Fig 7: Normalized gate trigger voltage as a function of junction temperature

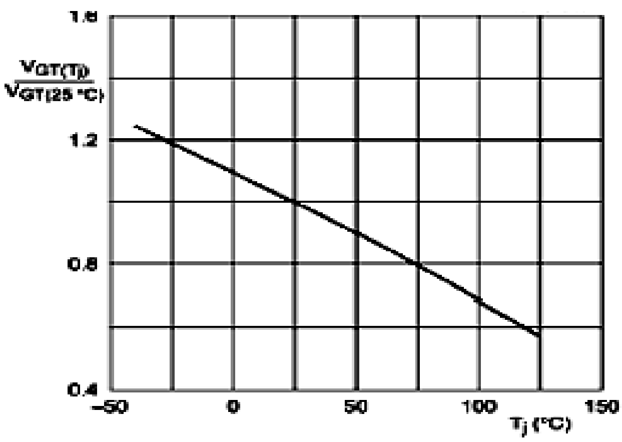
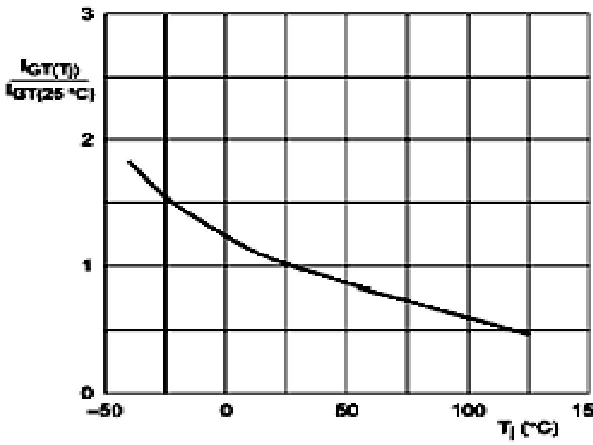


Fig 8: Normalized gate trigger voltage as a current of junction temperature



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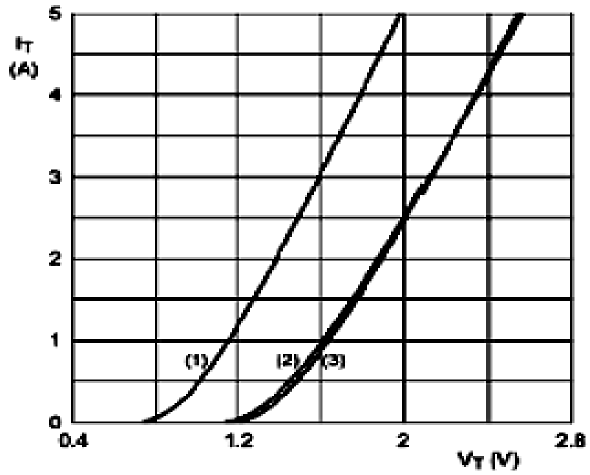
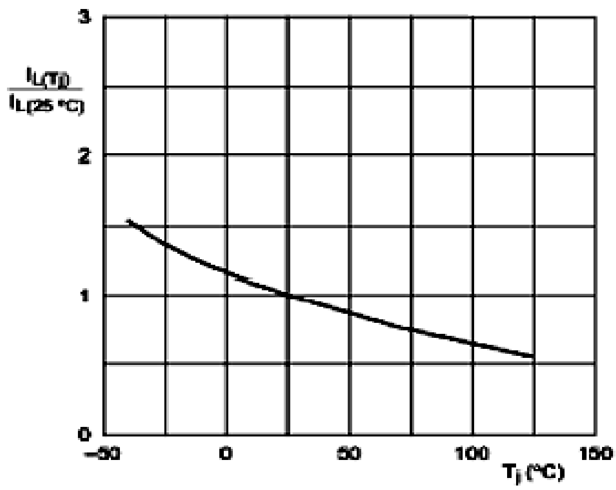
TYPICAL CHARACTERISTICS CURVES

Fig 9: On-state current characteristics



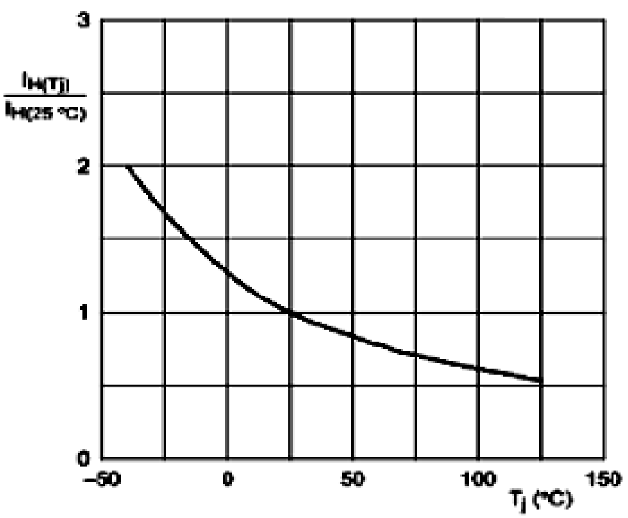
V_O = 1.067 V.
R_S = 0.187 Ω.
(1) T_j = 125 °C; typical values.
(2) T_j = 125 °C; maximum values.
(3) T_j = 25 °C; maximum values.

Fig 10: Normalized latching current as a function of junction temperature



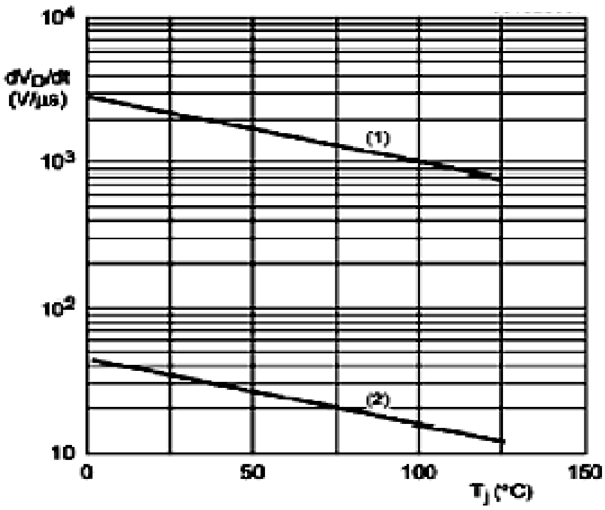
R_{GK} = 1 kΩ.

Fig 11: Normalized holding current as a function of junction temperature



R_{GK} = 1 kΩ.

Fig 12: Critical rate of rise of off-state voltage as a function of junction temperature; typical value



(1) R_{GK} = 1 kΩ.
(2) Gate open circuit.

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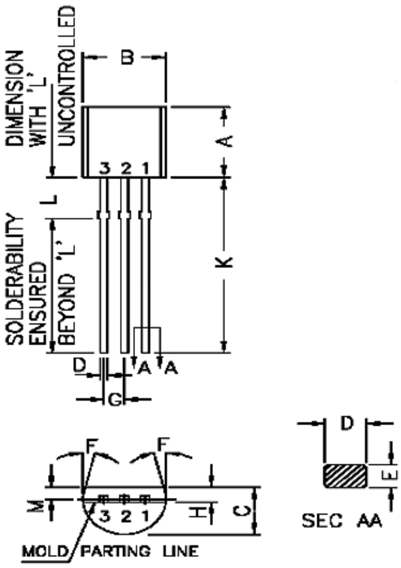
PACKAGE DETAILS

TO-92 Plastic Package

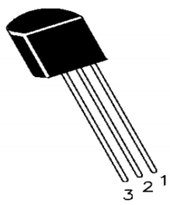


DIM	MIN	MAX
A	4,32	5,33
B	4,45	5,20
C	3,18	4,19
D	0,41	0,55
E	0,35	0,50
F	5 DEG	
G	1,14	1,40
H	1,20	1,40
K	12,70	--
L	1,982	2,082
M	1,03	1,20

All dimensions are in mm

PIN CONFIGURATION

1. ANODE
2. GATE
3. CATHODE



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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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