NPN SILICON PLANAR EPITAXIAL TRANSISTORS

MPS2222
MPS2222A

TO-92

TO-92
Plastic Package
RoHS compliant

FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATIONS: General Purpose Transistors

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	MPS2222	MPS2222A	UNIT
Collector Emitter Voltage	V_{CEO}	30	40	V
Collector Base Voltage	V_{CBO}	60	75	V
Emitter Base Voltage	V_{EBO}	5	6	V
Collector Current Continuous	I_C	600		mA
Power Dissipation@ Ta=25ºC	P_D	625		mW
Derate Above 25ºC		5.0		mW/°C
Power Dissipation@ Tc=25ºC	P_D	1.5		W
Derate Above 25ºC		12		mW/°C
Operating And Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150		°C

THERMAL RESISTANCE

Junction to Case	$R_{th\ (j\text{-}c)}$	83.3	°C/W
Junction to Ambient in free air	$R_{th\ (j\text{-}a)}$	200	°C/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	Min/ Max	MP S2222	MPS 2222A	UNIT
Collector Emitter Voltage	BV_{CEO}	I_C=10mA,I_B=0	Min	30	40	V
Collector Base Voltage	BV_{CBO}	I_C=10µA,I_E=0	Min	60	75	V
Emitter Base Voltage	BV_{EBO}	I_E=10µA, I_C=0	Min	5	6	V
Collector Cut off Current	I_{CEX}	V_{CE} =60V, V_{BE}=3.0V	Max	--	10	nA

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	Min/ Max	MP S2222	MPS 2222A	UNIT
Collector Cut off Current	I_{CBO}		Max	0.01	--	μA
		V_{CB}=50V, I_E = 0	Max	--	0.01	μA
		V_{CB}=60V, I_E = 0	Max	10	--	μA
		V_{CB}=50V, I_E = 0, Ta= 125ºC	Max	--	10	μA
		V_{CB}=60V, I_E = 0, Ta= 125ºC		--	--	
Emitter Cut off Current	I_{EBO}	V_{BE}=3V, I_C = 0	Max	--	10	nA
Base Cut off Current	I_{BL}	V_{CE}=60V,V_{BE}=3.0V	Max	--	20	nA
DC Current Gain	h_{FE}	V_{CE}=10V,I_C=0.1mA	Min	35	35	
		V_{CE}=10V,I_C=1mA	Min	50	50	
		V_{CE}=10V,I_C=10mA	Min	75	75	
		V_{CE}=10V,I_C=10mA,T_A=-55 ºC	Min	--	35	
		V_{CE}=10V [1],I_C=150mA		100~300	100~300	
		V_{CE}=1V [1],I_C=150mA	Min	50	50	
		V_{CE}=10V [1],I_C=500mA	Min	30	40	
Base Emitter Saturation Voltage	$V_{BE(sat)}$ [1]	I_C=150mA,I_B=15mA	Min	1.3	0.6~1.2	V
		I_C=500mA,I_B= 50mA	Min	2.6	2.0	V
Collector Emitter Saturation Voltage	$V_{CE\ (sat)}$ [1]	I_C=150mA,I_B=15mA	Min	0.4	0.3	V
		I_C=500mA,I_B=50mA	Min	1.6	1.0	V
DYNAMIC CHARACTERISTICS						
Transition Frequency	f_T	I_C=20mA, V_{CE}=20V, f=100MHz	Min	250	300	MHz
Output Capacitance	C_{ob}	I_E=0, V_{CB}=10V, f=1MHz	Max	--	8	pF
Input Capacitance	C_{ib}	Ic=0, V_{EB}=0.5V, f=1MHz	Max	30	25	pF
Input Impedance	h_{ie}	I_C=1mA, V_{CE}=10V, f=1KHz		--	2.0~8.0	KW
		I_C=10mA, V_{CE}=10V, f=1KHz		--	0.25~1.25	KW
Reverse Voltage Transfer Ratio	h_{re}	I_C=1mA, V_{CE}=10V, f=1KHz	Max	--	8	x 10^{-4}
		I_C=10mA, V_{CE}=10Vf=1KHz	Max	--	4	x 10^{-4}
Output Admittance	h_{oe}	I_C=1mA, V_{CE}=10Vf=1KHz		--	5~35	μMHO
		I_C=10mA, V_{CE}=10Vf=1KHz		--	25~200	μMHO
Noise Figure	NF	V_{CE} =10V,I_C=100uA, RS=1KOHMS,f=1KHZ	Max	--	4	dB
Collector Base Time Constant	rb' Cc	V_{CE} =20V,I_C=20mA,f=31.8MHZ	Max	--	150	ps
Small Signal Current Gain	| h_{fe} |	V_{CE} =10V,I_C=1mA, f=1KHZ		--	50~300	
		V_{CE} =10V,I_C=10mA, f=1KHZ		--	75~375	
SWITCHING CHARCTERISTIC						
Delay Time/Rise Time	t_d	V_{CC} =30V, V_{EB} =0.5V	Max	--	10	ns
	t_r	I_C =150mA, I_{B1}= 15mA	Max	--	25	ns
Storage Time/Fall Time	t_s	I_C =150mA, I_{B1}= I_{B2} 15mA	Max	--	225	ns
	t_f	V_{CC} =30V	Max	--	60	ns

Note:

1. Pulse Condition: = Width ≤ 300us, Duty Cycle ≤ 2%.

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Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

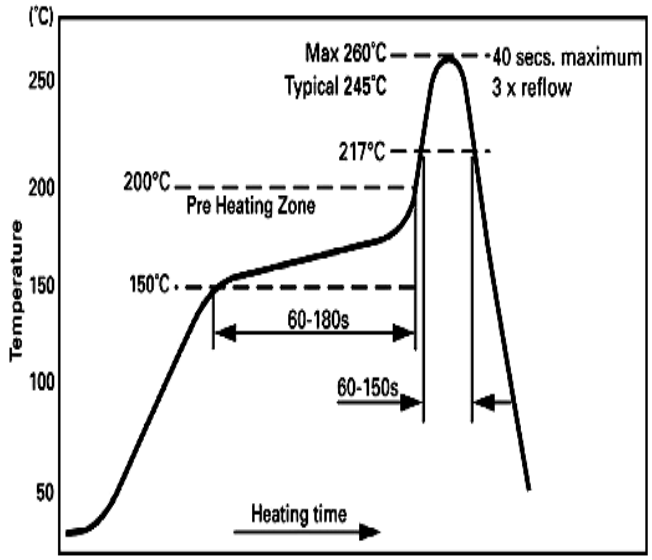
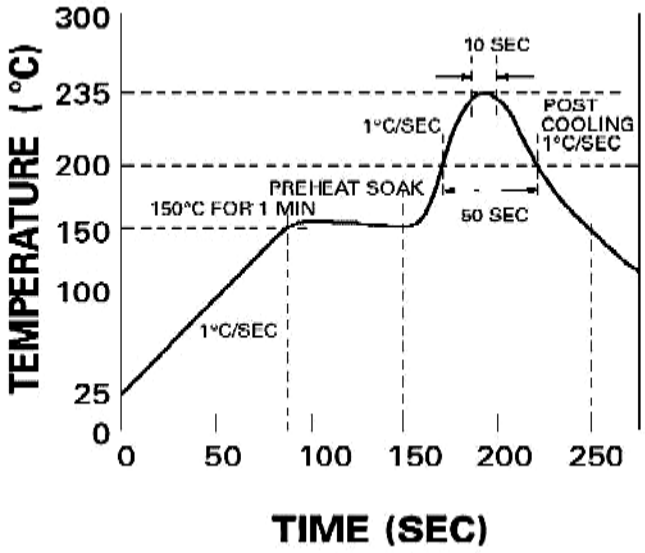


Figure 2

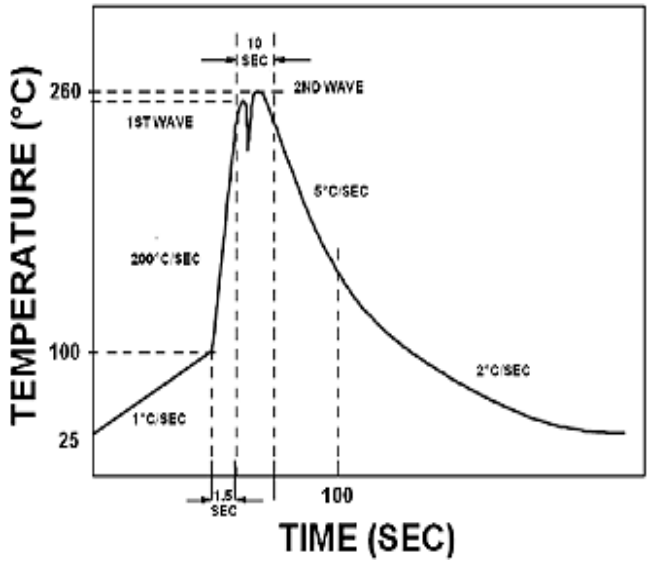


Reflow profiles in tabular form

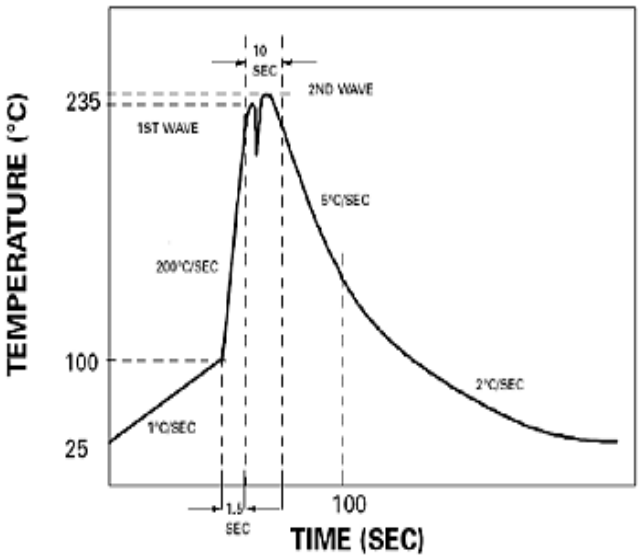
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Turn–On Time

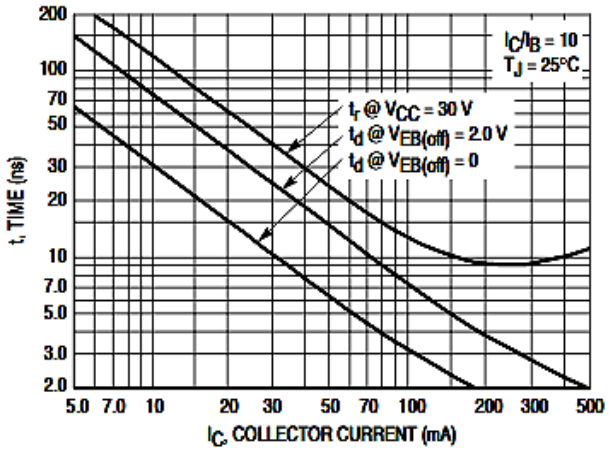


Fig 2: Frequency Effects

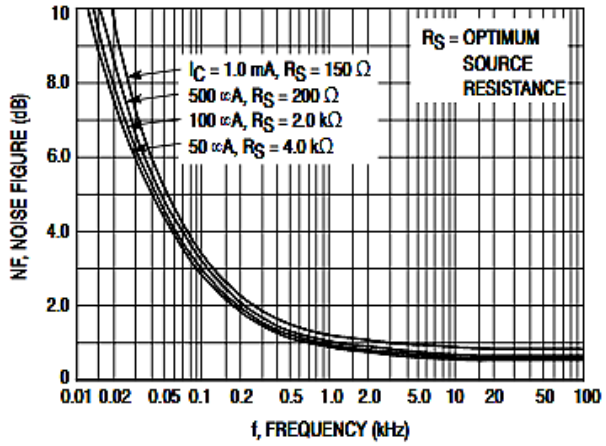


Fig 3: Capacitance

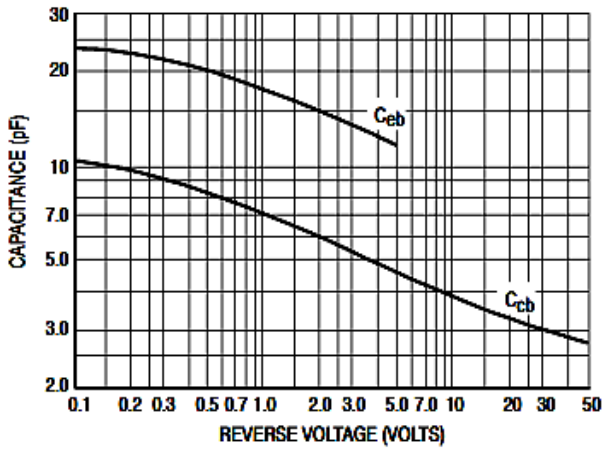


Fig 4: Turn–Off Time

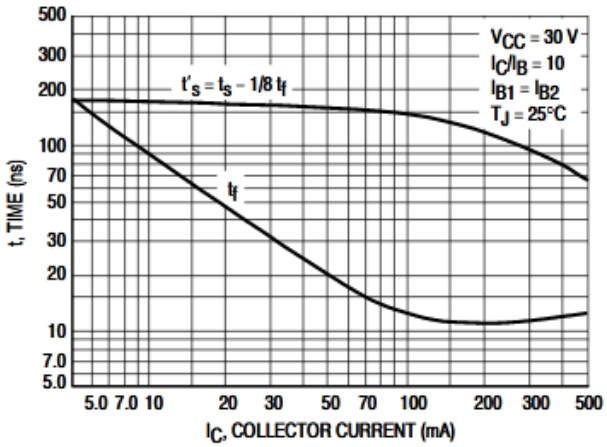


Fig 5: Source Resistance Effects

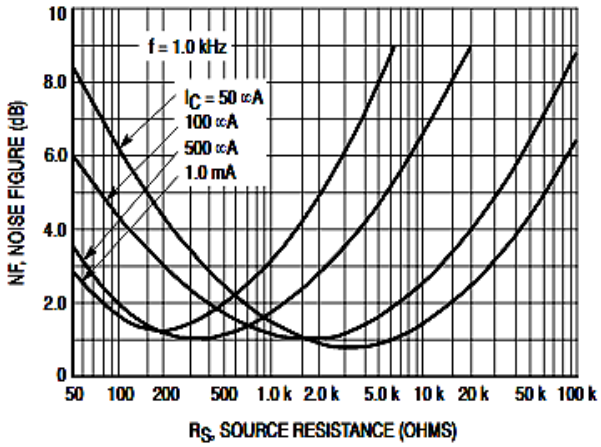
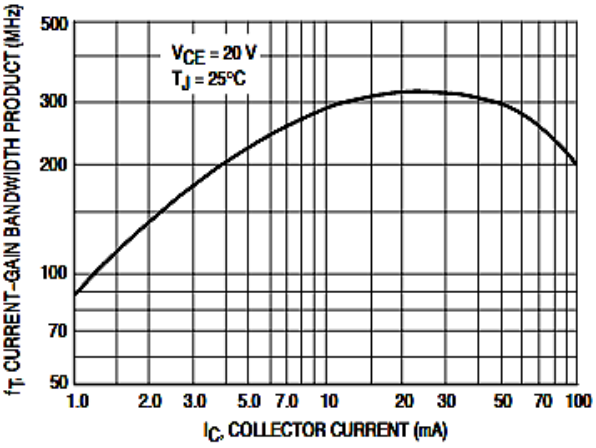


Fig 6: Current–Gain Bandwidth Product



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TYPICAL CHARACTERISTICS CURVES

Fig 7: “On” Voltages

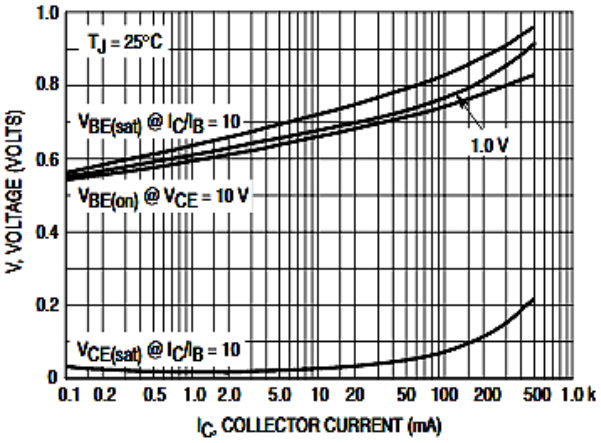


Fig 8: Temperature Coefficients

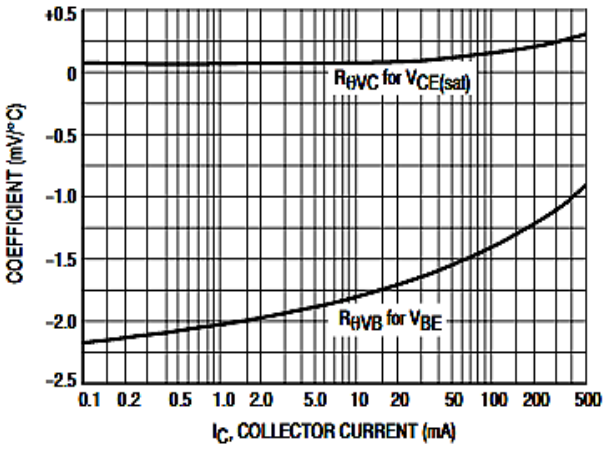


Fig 9: DC Current Gain

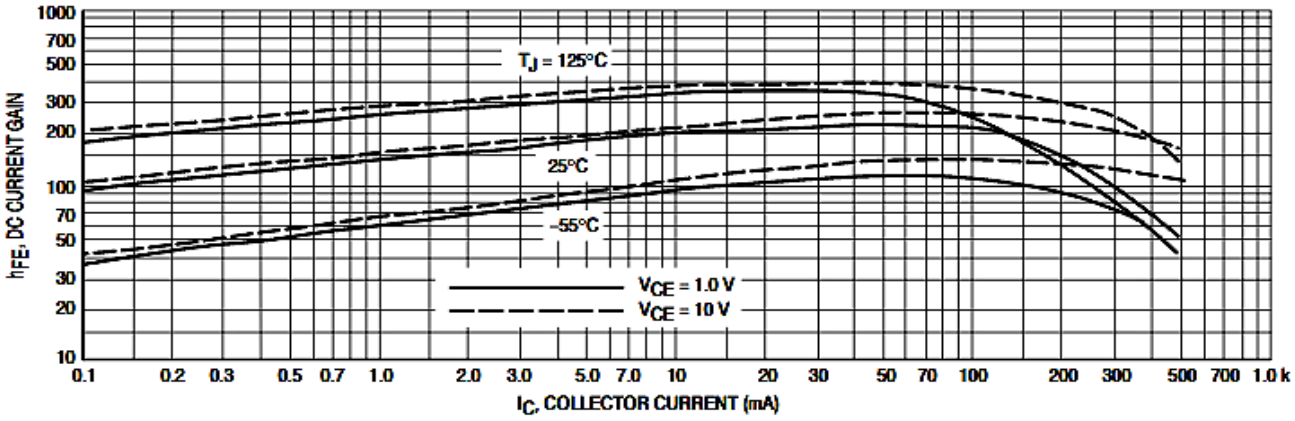
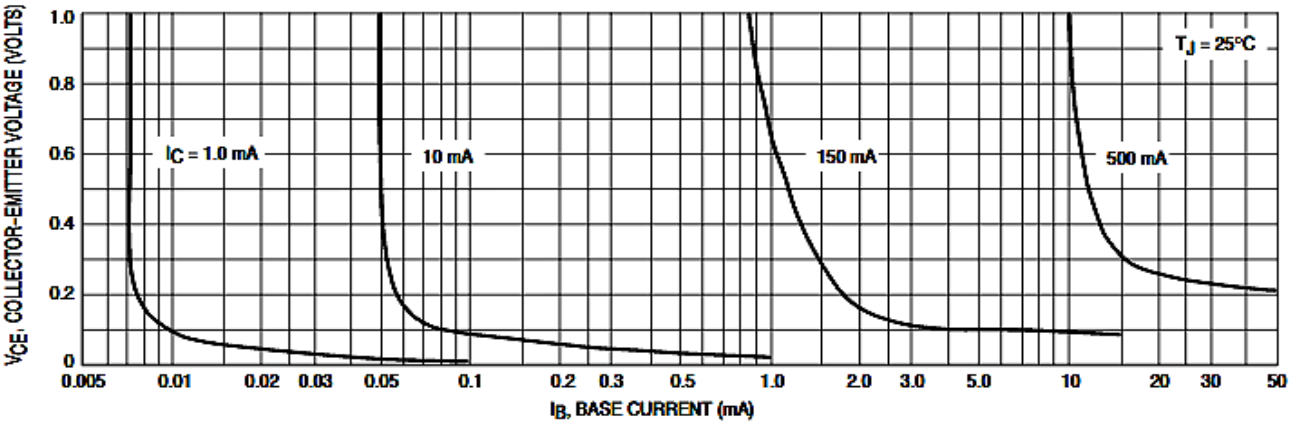
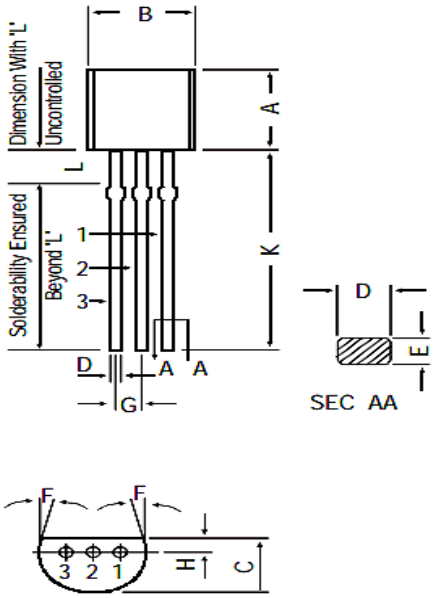


Fig 10: Collector Saturation Region



PACKAGE DETAILS

TO-92 Leaded Plastic Package

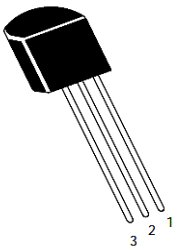


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5°	
G	1.14	1.40
H	1.14	1.53
K	12.70	
L	1.982	2.082

All dimensions are in mm

PIN CONFIGURATION

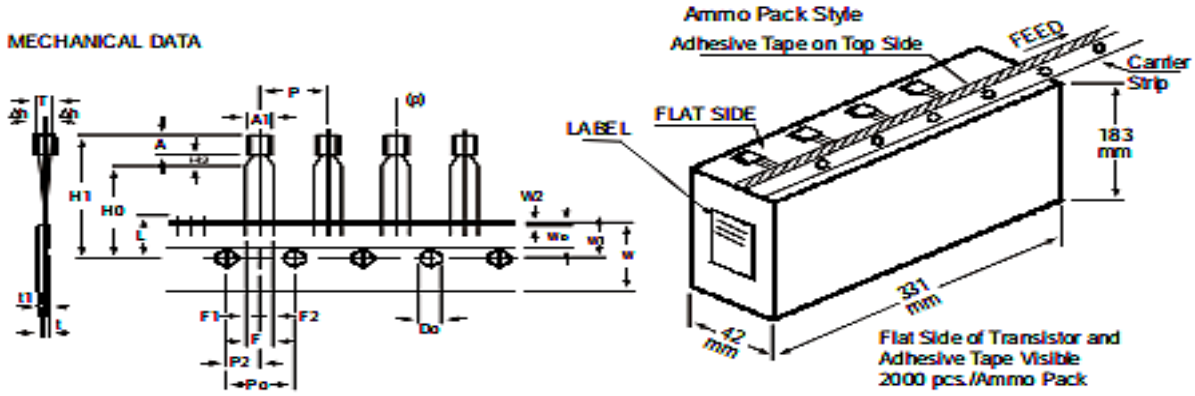
1. Collector
2. Base
3. Emitter



Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5K	17" x 15" x 13.5"	80K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2K	17" x 15" x 13.5"	32K	12.5 kgs

TO-92 Transistors on Tape and Ammo Pack



All dimensions in mm unless specified otherwise

ITEM	SYMBOL	SPECIFICATION				REMARKS
		MIN.	NOM.	MAX.	TOL.	
BODY WIDTH	A1	4.0		4.8		
BODY HEIGHT	A	4.8		5.2		
BODY THICKNESS	T	3.9		4.2		
PITCH OF COMPONENT	P		12.7		±1	
FEED HOLE PITCH	Po		12.7		±0.3	CUMULATIVE PITCH ERROR 1.0 mm/20 PITCH
FEED HOLE CENTRE TO COMPONENT CENTRE	P2		6.35		±0.4	TO BE MEASURED AT BOTTOM OF CLINCH
DISTANCE BETWEEN OUTER LEADS	F		5.08		+0.6 -0.2	
COMPONENT ALIGNMENT	Δh		0	1		AT TOP OF BODY
TAPE WIDTH	W		18		±0.5	
HOLD-DOWN TAPE WIDTH	Wo		6		±0.2	
HOLE POSITION	W1		9		+0.7 -0.5	
HOLD-DOWN TAPE POSITION	W2		0.5		±0.2	
LEAD WIRE CLINCH HEIGHT	Ho		16		±0.5	
COMPONENT HEIGHT	H1			23.25		
LENGTH OF SNIPPED LEADS	L			11.0		
FEED HOLE DIAMETER	Do		4		±0.2	
TOTAL TAPE THICKNESS	t			1.2		t1 0.3 - 0.6
LEAD - TO - LEAD DISTANCEF1,	F2		2.54		+0.4 -0.1	
CLINCH HEIGHT	H2			3		
PULL - OUT FORCE	(P)	6N				

NOTES

1. MAXIMUM ALIGNMENT DEVIATION BETWEEN LEADS NOT TO BE GREATER THAN 0.2 mm
2. MAXIMUM NON-CUMULATIVE VARIATION BETWEEN TAPE FEED HOLES SHALL NOT EXCEED 1 mm IN 20 PITCHES.
3. HOLDDOWN TAPE NOT TO EXCEED BEYOND THE EDGE(S) OF CARRIER TAPE AND THERE SHALL BE NO EXPOSURE OF ADHESIVE
4. NO MORE THAN 3 CONSECUTIVE MISSING COMPONENTS ARE PERMITTED.
5. A TAPE TRAILER, HAVING AT LEAST THREE FEED HOLES ARE REQUIRED AFTER THE LAST COMPONENT.
6. SPLICES SHALL NOT INTERFERE WITH THE SPROCKET FEED HOLES.

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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