

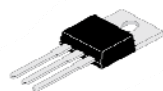


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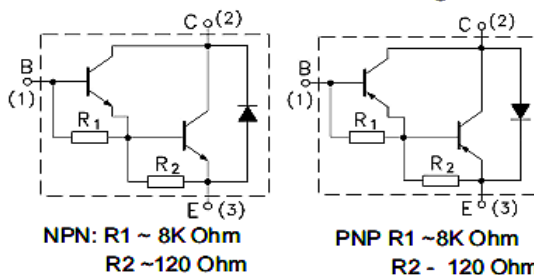


DARLINGTON PLASTIC POWER TRANSISTORS



TO-220

Internal Schematic Diagram



TIP120 TIP125
TIP121 TIP126
TIP122 TIP127
NPN PNP

TO-220
Plastic Package
RoHS compliant

FEATURES:

This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATIONS:

High Power Switching, Hammer Drive, Pulse Motor Drive and Inductive Load Drive

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TIP120/125	TIP121/126	TIP122/127	UNIT
Collector Emitter Voltage	V_{CEO}	60	80	100	V
Collector Base Voltage	V_{CBO}	60	80	100	V
Emitter Base Voltage	V_{EBO}	5			V
Collector Current Continuous	I_C	5			A
Collector Current Peak	I_{CM}	8			A
Base Current	I_B	120			mA
Power Dissipation upto Tc=25°C	P_D	65			W
Derate above 25°C		0.52			W/°C
Power Dissipation upto Ta=25°C	P_D	2			W
Derate above 25°C		16			W/°C
Unclamped Inductive Load Energy	E^1	50			mJ
Operating And Storage Junction Temperature	T_j, T_{stg}	-65 to +150			°C

THERMAL RESISTANCE

Junction to Case	$R_{th(j-c)}$	1.92	°C/W
Junction to Ambient in free air	$R_{th(j-a)}$	62.5	°C/W

TIP120_127
Rev02_ 10062022EM



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ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise

PARAMETER	SYMBOL	TEST CONDITION	TIP120/125		TIP121/126		TIP122/127		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Collector Emitter (sus) Voltage	$V_{CE(sus)}$	$I_C=100mA, I_B=0$	60	--	80	--	100	--	V
Collector Cut Off Current	I_{CEO}	$V_{CE}=50V, I_B=0$	--	--	--	--	--	0.5	mA
		$V_{CE}=40V, I_B=0$	--	--	--	0.5	--	--	
		$V_{CE}=30V, I_B=0$	--	0.5	--	--	--	--	
Collector Cut Off Current	I_{CEO}	$V_{CB}=100V, I_E=0$	--	--	--	--	--	0.2	mA
		$V_{CB}=80V, I_E=0$	--	--	--	0.2	--	--	
		$V_{CB}=60V, I_E=0$	--	0.2	--	--	--	--	
Emitter Cut Off Current	I_{EBO}	$V_{EB}=5V, I_C=0$	--	2.0	--	2.0	--	2.0	
DC Current Gain	h_{FE}	$I_C=0.5A, V_{CE}=3V$	1000	--	1000	--	1000	--	
		$I_C=3A, V_{CE}=3V$	1000	--	1000	--	1000	--	
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=3A, I_B=12mA$	--	2.0	--	2.0	--	2.0	V
		$I_C=5A, I_B=20mA$	--	4.0	--	4.0	--	4.0	
Base Emitter On Voltage	$V_{BE(on)}$	$I_C=3A, V_{CE}=3V$	--	2.5	--	2.5	--	2.5	V

DYNAMIC CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
Small Signal Current Gain	h_{fe}	$I_C=3A, V_{CE}=4V, f=1MHz$	4			
Output Capacitance	C_{ob}	$V_{CB}=10V, I_E=0, f=0.1MHz$				
		TIP125,126,127			300	pF
		TIP120,121,122			200	pF

SWITCHING CHARACTERISTICS

Turn on time	t_{on}	$I_C=3A, R_L=10W$ $I_{B1}=I_{B2}=12mA$ $V_{EB(off)}=5V$		0.4		μs
Turn off time	t_{off}			1.2		μs

Note:

- $I_C=1A, L=100mH, P.R.F.=10Hz, V_{cc}=20V, R_{BE}=100\Omega$
- Pulse Test : Pulse width <300ms, Duty Cycle <2%
- For PNP device voltage and current values will be negative (-).

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

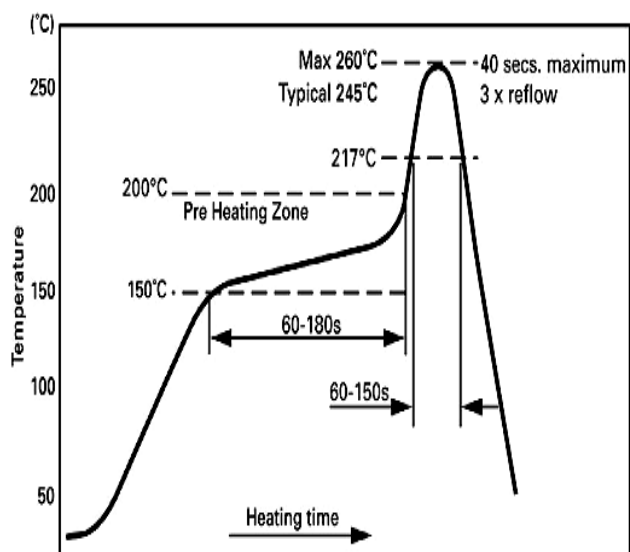
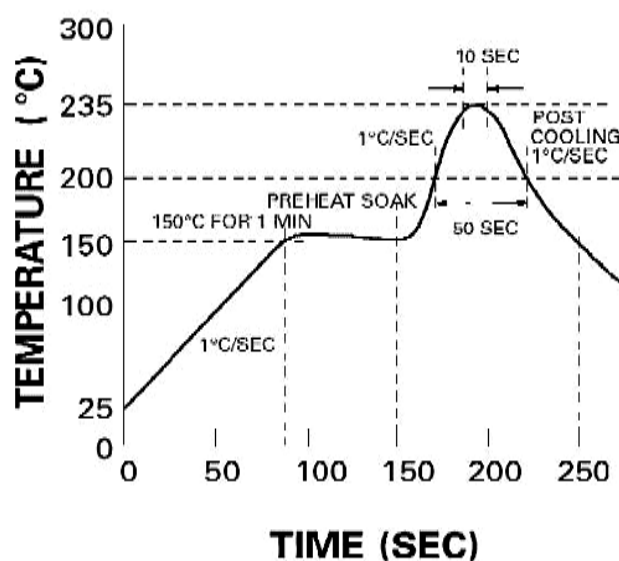


Figure 2



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Time	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.



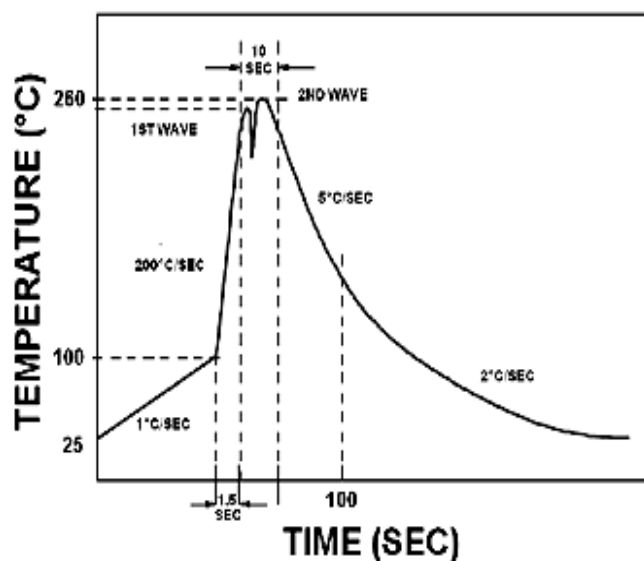
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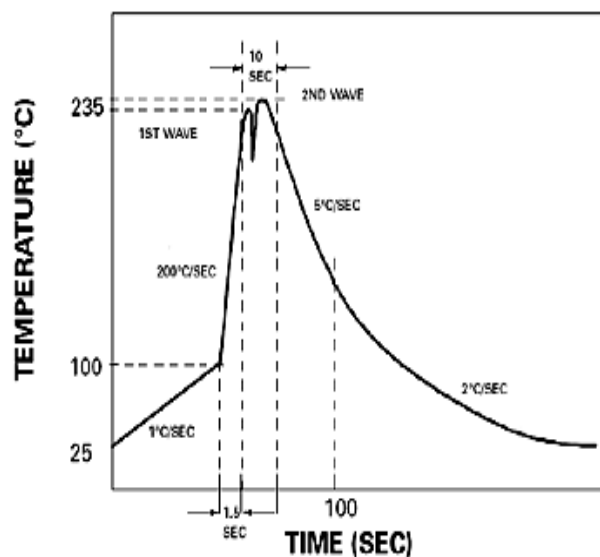


Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Safe operating area

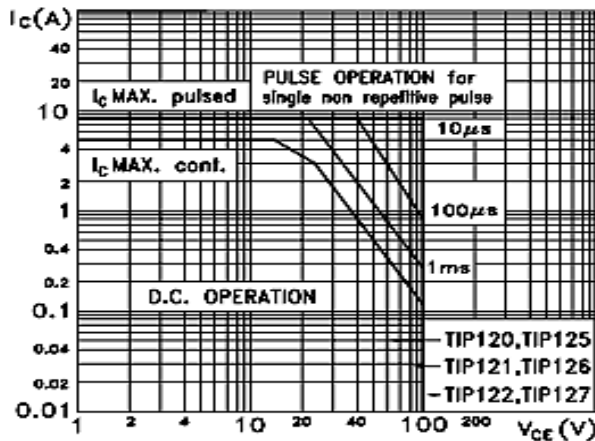


Fig 2: DC current gain for NPN type

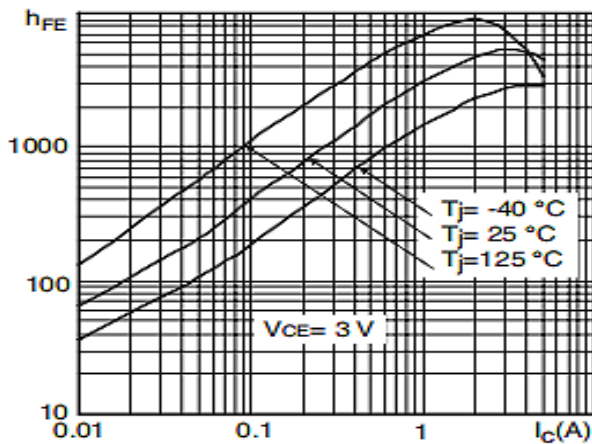


Fig 3: Collector-emitter saturation voltage for NPN type

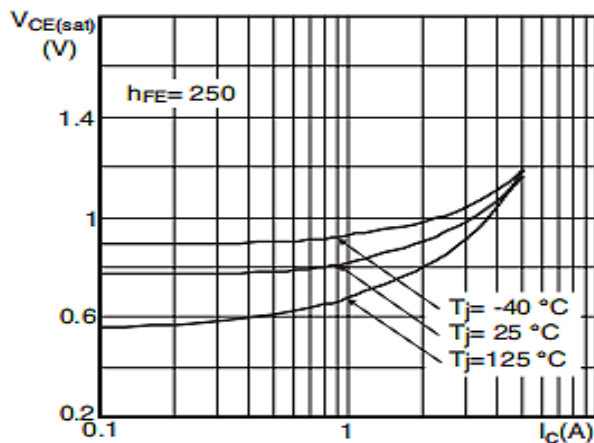


Fig 4: Derating curve

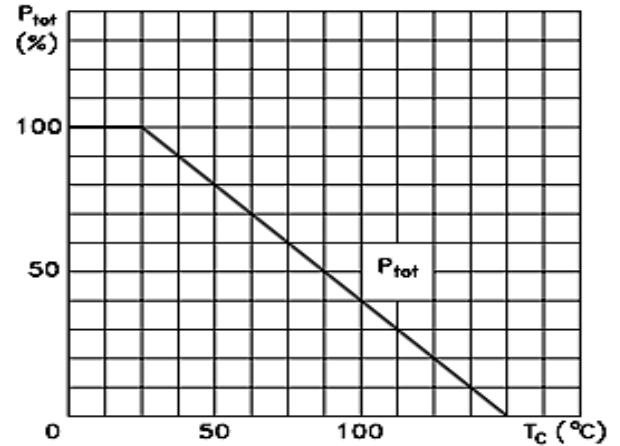


Fig 5: DC current gain for PNP type

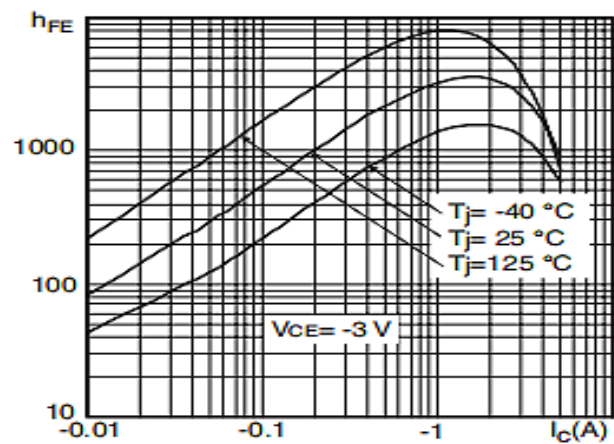
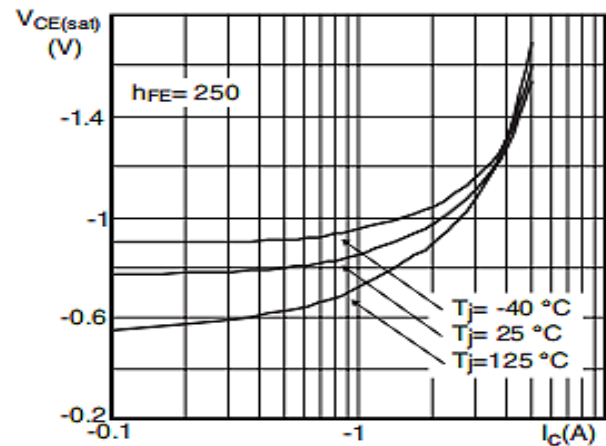


Fig 6: Collector-emitter saturation voltage for PNP type



TYPICAL CHARACTERISTICS CURVES

Fig 7: Base-emitter saturation voltage for NPN type

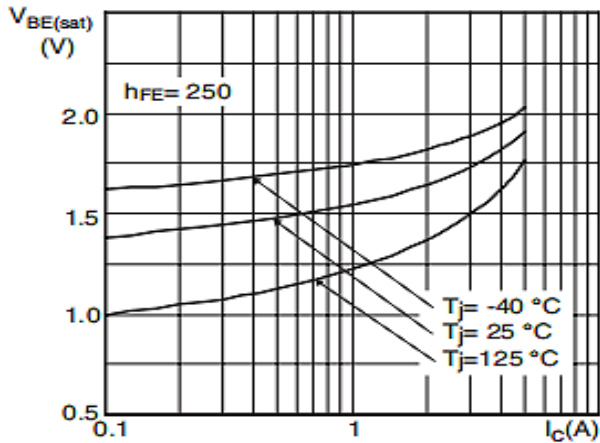


Fig 8: Base-emitter on voltage for NPN type

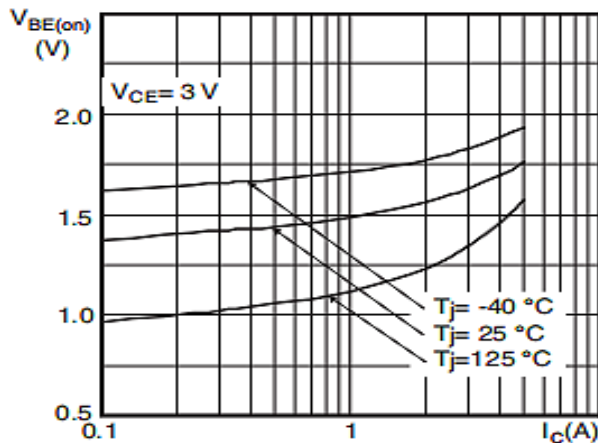


Fig 9: Switching time on resistive load for NPN type (on)

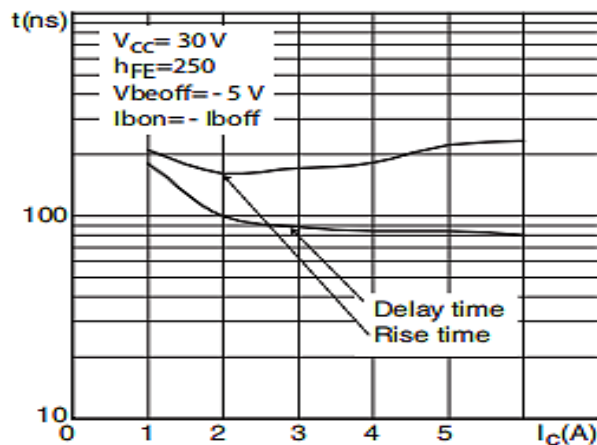


Fig 10: Base-emitter saturation voltage for PNP type

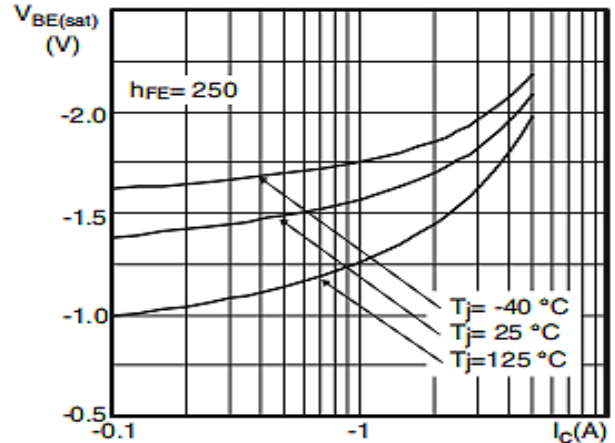


Fig 11: Base-emitter on voltage for PNP type

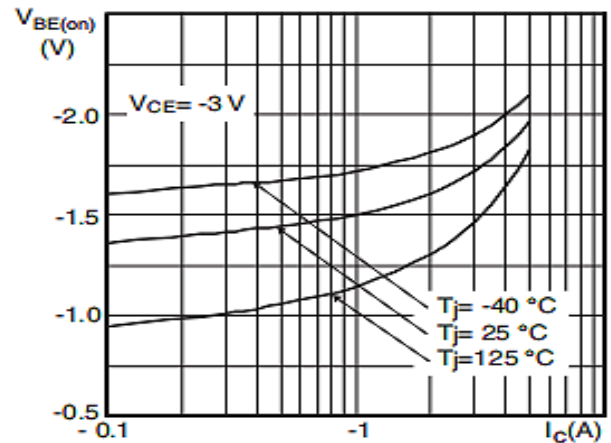
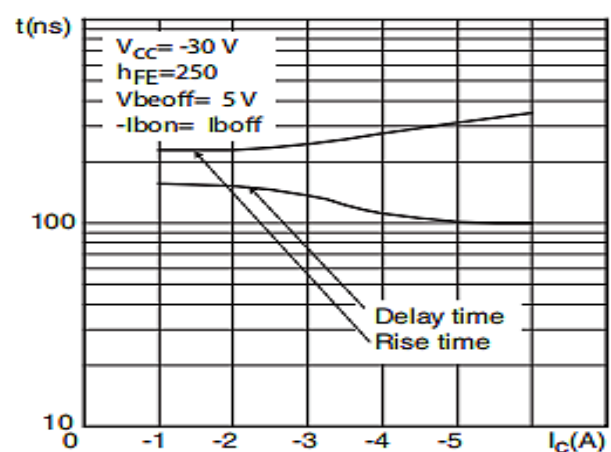


Fig 12: Switching time on resistive load for PNP type (on)



TYPICAL CHARACTERISTICS CURVES

Fig 13: Switching time on resistive load for NPN type (off)

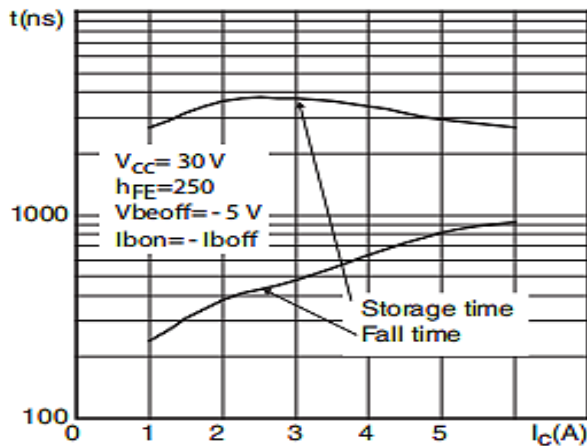


Fig 14: Capacitance for NPN type

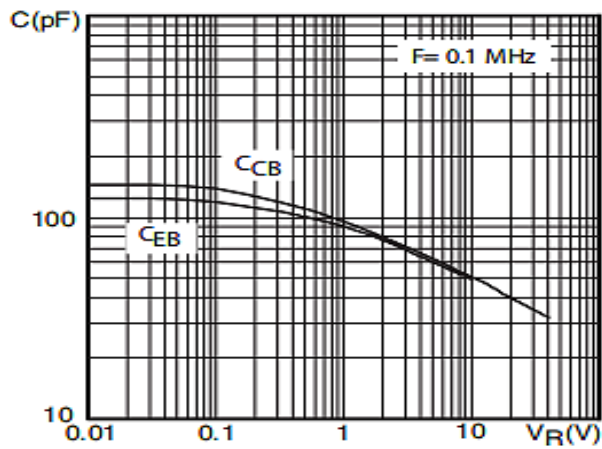


Fig 15: Switching time on resistive load for PNP type (off)

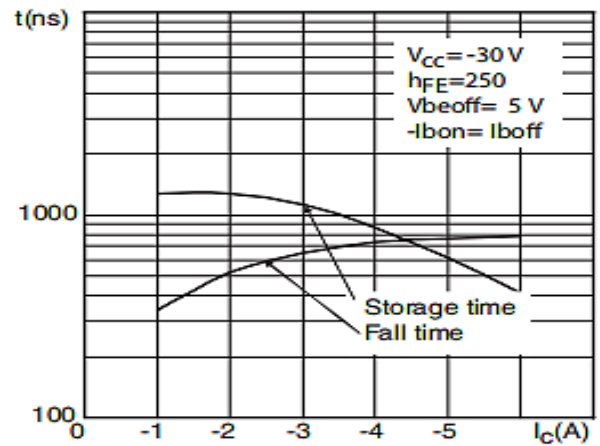
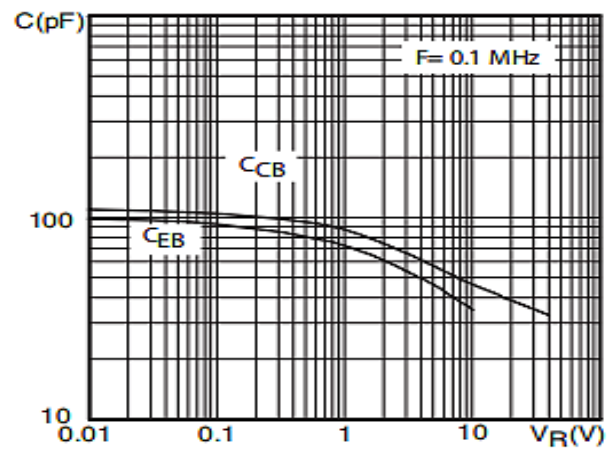
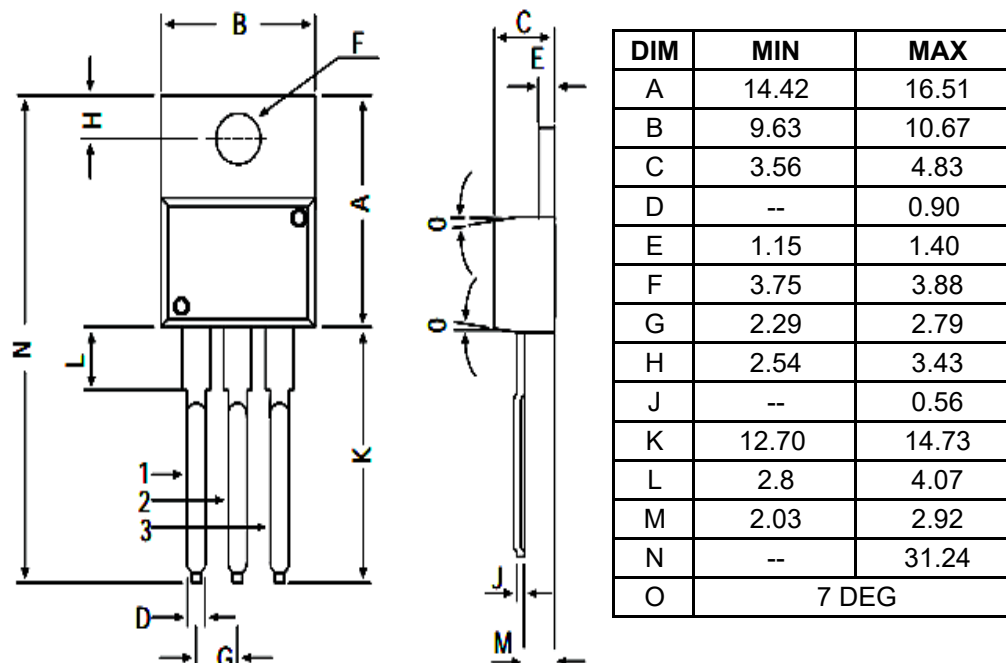


Fig 16: Capacitance for PNP type



PACKAGE DETAILS

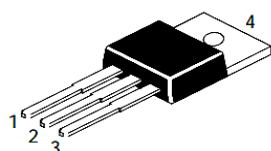
TO-220 Plastic Package



All dimensions in mm.

Pin Configuration

1. Base
2. Collector
3. Emitter
4. Collector



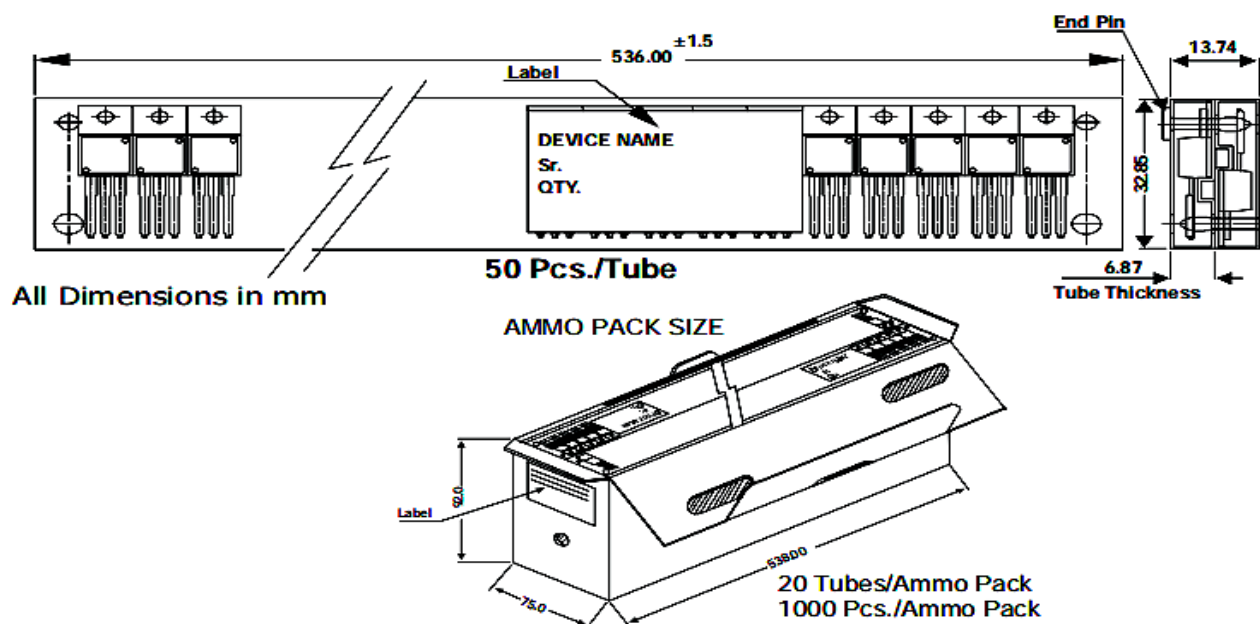


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TO-220 Tube Packing



Packing Detail

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-220	200 pcs/polybag	396 gm/200 pcs	3' x 7.5' x 7.5'	1.0K	17' x 15' x 13.5'	16.0K	36 kgs
	50 pcs/tube	120 gm/50 pcs	3.5' x 3.7' x 21.5'	1.0K	19' x 19' x 19'	10.0K	29 kgs

TIP120_127

Rev02_ 10062022EM



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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
 - Humidity between 40 to 70 %RH
 - Air should be clean.
 - Avoid harmful gas or dust.
 - Avoid outdoor exposure or storage in areas subject to rain or water spraying .
 - Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
 - Avoid rapid change of temperature.
 - Avoid condensation.
 - Mechanical stress such as vibration and impact shall be avoided.
 - The product shall not be placed directly on the floor.
 - The product shall be stored on a plane area. They should not be turned upside down.
- They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information.

Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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TIP120_127

Rev02_ 10062022EM